

INTEGRATED CIRCUIT HAVING A SYNCHRONOUS AND AN ASYNCHRONOUS CIRCUIT AND METHOD FOR OPERATING SUCH AN INTEGRATED CIRCUIT

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Background of the Invention:

Field of the Invention:

The present invention relates to an integrated circuit having a synchronous circuit and an asynchronous circuit and to a method for operating such an integrated circuit.

Integrated circuits often have synchronously operated and asynchronously operated circuit sections which are connected to one another for data exchange, for example. In this case, the synchronously operated circuit sections are clock-controlled, in other words there is generally a globally available clock signal present by means of which the operation of the synchronous circuit section is controlled time-synchronously. In contrast to this, an asynchronously operated circuit section is not clock-controlled. Integrated circuits constructed in this way are found for example in the field of memory circuits, such as for instance, in the field of so-called embedded DRAMs (Dynamic Random Access Memories). In this case, by way of example, a DRAM memory circuit which essentially operates asynchronously is contained in an

integrated circuit which additionally has synchronous circuit sections.

If different circuits which operate synchronously with respect
5 to a clock signal and asynchronously, respectively, are used
in an integrated circuit, then it is necessary to provide
defined interfaces between the different circuits concerned.

Clock-controlled register circuits are usually used for this
purpose. In this case, data from a synchronous circuit are
10 stored in an input register circuit with, for example, the
rising edge of the clock signal. The data are transferred from
the input register circuit into the relevant asynchronous
circuit, the data are processed in the asynchronous circuit
and forwarded to an output register circuit, into which the
15 data are accepted upon the next rising edge of the clock
signal. The data of the output register are transferred to the
synchronous circuit for further processing.

In this case, difficulties may occur in particular if the data
20 processing duration of the asynchronous circuit is longer than
the period duration of the clock signal. This is because the
input data for the asynchronous circuit that are to be stored
in the input register circuit can change with the next rising
edge of the clock signal. For proper operation of the
25 integrated circuit, the input data must remain the same
throughout the processing time of the asynchronous circuit, in

order to ensure correct processing by the asynchronous circuit. In order to hold the input data for a plurality of clock cycles, it is necessary, for example, to provide an additional register in the synchronous circuit.

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If it is established in this case, for example, that the synchronous circuit further processes the data from the output register circuit only after a defined number of clock cycles, this can have the effect that the synchronous circuit has to wait for an unnecessarily long time for the processed data of the asynchronous circuit for further processing. This can occur primarily in the case of variable clock frequencies of the synchronous circuit and can limit the data throughput.

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Summary of the Invention:

It is accordingly an object of the invention to provide an integrated circuit having a synchronous circuit and an asynchronous circuit, and a method of operating the integrated circuit which overcomes the above-mentioned disadvantages of the prior art apparatus and methods of this general type. In particular, it is an object of the invention to provide an integrated circuit which enables a relatively high data throughput between the synchronous circuit and the asynchronous circuit.

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With the foregoing and other objects in view there is provided, in accordance with the invention, an integrated circuit, that includes: a synchronous circuit; an asynchronous circuit; an input register circuit connected to the 5 synchronous circuit and the asynchronous circuit, the input register circuit having a terminal receiving a first control clock signal for controlling data transfer; an output register circuit connected to the synchronous circuit and the asynchronous circuit, the output register circuit having a terminal receiving a second control clock signal for controlling data transfer; and a sequence controller. The synchronous circuit stores data in the input register circuit so that the data can be processed in the asynchronous circuit. The asynchronous circuit stores the processed data in the output register circuit so that the processed data can be further processed in the synchronous circuit. The sequence controller is connected to the asynchronous circuit for generating the first control clock signal and the second control clock signal in dependence on a duration required for 20 the data to be processed in the asynchronous circuit.

With the foregoing and other objects in view there is also provided, in accordance with the invention, a method for operating the inventive integrated circuit, in which the first control clock signal is activated for the purpose of transferring data from the synchronous circuit into the input

register circuit, the data are transferred from the input register circuit into the asynchronous circuit and are processed in the asynchronous circuit, the first control clock signal is inactivated by the sequence controller within the 5 data processing duration of the asynchronous circuit, and in which the second control clock signal, at or after the end of the data processing duration of the asynchronous circuit, triggers transfer of the processed data into the output register circuit.

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The integrated circuit and the operating method enable a comparatively high data throughput between the synchronous circuit and the asynchronous circuit. The data exchange between the asynchronous circuit and the synchronous circuit is adapted to the processing speed of the asynchronous circuit. This means, for example, that the synchronous circuit does not have to wait for a previously defined number of clock cycles for the result of the asynchronous circuit, which lowers the data throughput.

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The fact that the first control clock signal is deactivated within the data processing duration of the asynchronous circuit avoids the situation in which data stored in the input register circuit are overwritten by new data of the 25 synchronous circuit, as long as the asynchronous circuit has not yet concluded the processing of the old data. The fact

that the second control clock signal, at or after the end of the data processing duration, triggers the transfer of the processed data into the output register circuit enables the further processing of the data to be carried out by the 5 synchronous circuit immediately after the end of the processing in the asynchronous circuit. Besides the relatively high data throughput, in addition, a relatively simple design of the integrated circuit is made possible since there is no need for additional registers or circuits for holding or buffer-storing the input data.

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In accordance with an added feature of the invention, the integrated circuit has a terminal for a clock signal, the terminal for the clock signal and the terminal for the first control clock signal are connected to one another via a controllable switching means. For generation of the first control clock signal, the controllable switching means can be controlled by the sequence controller. If the switching means is closed, then the clock signal forms the first control clock signal. If the switching means is open, then the first control clock signal is switched off or deactivated. This means that the integrated circuit itself switches off the first control clock signal by means of the sequence controller, in order to hold the data stored in the input register circuit, in order 20 that the asynchronous circuit can carry out the data processing properly. The integrated circuit additionally 25

determines, by means of the sequence controller, the instant that the data is output from the asynchronous circuit and the renewed switch-on of the first control clock signal.

5 Such a mode of operation of the integrated circuit is particularly advantageous for the case where the terminal for the clock signal is connected to the synchronous circuit for the purpose of controlling the operation of the synchronous circuit, and, in addition, the clock frequency of the clock signal is adjustable in a variable manner. A high data throughput is ensured in this case even in the event of an altered clock frequency of the clock signal and thus in the event of an altered data processing speed of the synchronous circuit. A comparatively slowly clocked design of the synchronous circuit can accept the data, for example, as early as after two clock periods, and a comparatively fast design of the synchronous circuit must wait for correspondingly more clock periods in order to accept the result of the asynchronous circuit. As a result, the data transfer between

20 the synchronous circuit and the asynchronous circuit is adapted to the processing speed of the asynchronous circuit even in the event of an altered clock frequency of the clock signal, whereby a high data throughput is always achieved.

25 The invention can be used for diverse kinds of integrated circuits. By way of example, the asynchronous circuit has a

memory circuit of the DRAM type. A comparatively high memory throughput is made possible with such a so-called embedded DRAM design. In addition, the integrated circuit can be used for the case where the asynchronous circuit has an 5 analog/digital converter, for example.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

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Although the invention is illustrated and described herein as embodied in an integrated circuit having a synchronous and an asynchronous circuit and method for operating such an integrated circuit, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, 20 however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 shows an embodiment of an integrated circuit having a synchronous circuit and an asynchronous circuit; and

5 Fig. 2 shows a timing diagram of signals of the integrated circuit shown in Fig. 1.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an embodiment of an integrated circuit 1 having a synchronous circuit 2 and an asynchronous circuit 3. An input register circuit 4 is connected to the synchronous circuit 2 and the asynchronous circuit 3. An output register circuit 5 is likewise connected to the synchronous circuit 2 and the asynchronous circuit 3. Data DA1 of the synchronous circuit 2, which are to be processed further in the asynchronous circuit 3, are stored in the input register circuit 4. The processed data DA2 of the asynchronous circuit 3 are stored in the 20 output register circuit 5 in order to be processed further in the synchronous circuit 2. The asynchronous circuit 3 has a DRAM memory circuit 8 in this example.

The input register circuit 4 and the output register circuit 5 are clock-controlled in each case. The transfer of the data DA1 from the synchronous circuit 2 into the input register

circuit 4 is controlled by means of the control clock signal C1, which is present at the input register circuit 4 for this purpose. The transfer of the data DA2 from the asynchronous circuit 3 into the output register circuit 5 is controlled by 5 means of the control clock signal C2, which is present at the output register circuit 5 for this purpose.

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The integrated circuit 1 additionally has a terminal for a clock signal CK which controls the operation of the synchronous circuit 2. The terminal for the clock signal CK is connected to the synchronous circuit 2, and, in addition, the terminal for the clock signal CK is connected to the terminal for the control clock signal C1 via the switch 7. The switch 7 can be controlled by the sequence controller 6 that is connected to the asynchronous circuit 3. The sequence controller 6 generates a control signal W for controlling the switch 7, and, in addition, generates the control clock signal C2 for controlling the output register circuit 5.

20 Fig. 2 shows a timing diagram of the circuit shown in Fig. 1. The data DA1 are formed by the input data A, B, C and D. At the beginning of the data transfer from the synchronous circuit 2 into the asynchronous circuit 3, the switch 7 shown in Fig. 1 is closed. In order to transfer the data DA1 in the 25 form of the input data B from the synchronous circuit 2 into the input register circuit 4, the control clock signal C1 has

an active state (active high) at the instant t_1 . The input data B are stored in the input register circuit 4 as data D4. If the sequence controller 6 recognizes from the input data B, for example from a command, that the data processing in the 5 asynchronous circuit will take a comparatively long time, it switches off the control clock signal C1 for the input register circuit 4. To that end, the control signal W is put into an active state (active high). The consequence of this is that, in contrast to the clock period P1, in the clock period P2, no input data are transferred into the input register circuit 4. The "old" data D4 are still stored in the input register circuit 4 in order to be processed by the asynchronous circuit 3. To that end, the data D4 are transferred from the input register circuit 4 into the asynchronous circuit 3 and processed in the latter. On account of the control signal W, the control clock signal C1 is deactivated within the data processing duration TD of the asynchronous circuit 3.

20 Once the data have been completely processed in the asynchronous circuit 3, a clock pulse is generated in the form of the control clock signal C2 for the output register circuit 5. In addition, the signal W is switched back into its inactive state. The control clock signal C2 can be activated 25 at or after the end of the data processing duration TD of the asynchronous circuit 3 (instant t_2). The data DA2 are

transferred in the form of the processed output data E into the output register circuit 5 and stored (data D5). From the instant t2, the output data E are valid for further processing in the synchronous circuit 2.

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The invention avoids the situation in which, in particular, the output data E are transferred into the output register circuit 5 within the data processing duration TD and can thus assume an undefined state. This is advantageous in particular when the clock frequency of the clock signal CK is adjustable in a variable manner.

The control clock signal C1 is deactivated by opening the switch 7 by means of the activated control signal W. When the control signal W is deactivated, care must be taken to ensure that no additional pulses arise on the control clock signal C1 for the input register circuit 4. For this reason, the signal W is deactivated in the inactive phase (low phase) of the clock signal CK and the switch 7 is closed in the inactive state of the clock signal CK. For the control of such a time sequence, the sequence controller 6 is connected to the terminal for the clock signal CK.

In the embodiment shown, the sequence controller 6 is arranged outside the asynchronous circuit 3. In a further embodiment of the integrated circuit, however, it is also possible for the

sequence controller to be contained in the asynchronous circuit. As a result, the data transfer is performed via the input register circuit 4 and the output register circuit 5 by the asynchronous circuit 3 itself.

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